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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,826	02/17/2004	Anand Murthy	ITL.1064US (P18031)	3751
21906	7590	09/20/2006	EXAMINER	
TROP PRUNER & HU, PC 1616 S. VOSS ROAD, SUITE 750 HOUSTON, TX 77057-2631			SMOOT, STEPHEN W	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/780,826	<b>Applicant(s)</b> MURTHY ET AL.	
	<b>Examiner</b> Stephen W. Smoot	<b>Art Unit</b> 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 12 May 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) 14-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 and 19-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

This Office action is in response to applicant's amendment received on 12 May 2006.

### *Election/Restrictions*

1. Claims 14-18 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply received on 20 October 2005.

### *Claim Objections*

2. Claims 1, 31 are objected to because of the following informalities:

In claim 1, line 4, change "an amorphous" to --the amorphous-- for proper antecedence to line 3; and

In claim 31, line 2, change "over" to --in place of-- for proper antecedence.

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 26-32 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for “forming a film of mobility enhancing material over a semiconductor substrate and over a gate electrode structure” (claim 26, lines 2-3) as shown in see Fig. 3, does not reasonably provide enablement for “selectively etching the material over the gate electrode structure without substantially etching the material over the substrate” (claim 26, lines 4-5). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims.

The specification does not reasonably provide enablement for selectively etching the material over the gate electrode structure without substantially etching the material over the substrate because the gate electrode structure (14, 16) as shown in Fig. 3 is also formed over the substrate (12). Accordingly, when the material over the gate electrode (14, 16) is etched, material that is over the substrate (12) is also being etched.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5, 11-12, 26-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Mizushima et al. (US 2002/0034864 A1).

As best understood, “material over the substrate” as claimed in claim 26 is being interpreted to mean material that is directly in contact with the substrate.

Referring to Figs. 12A-12D and paragraphs [0119] to [0149], Mizushima et al. disclose a method for forming MOS transistors that includes forming a gate structure (2, 6, 7, 8) over a substrate (1) and then forming a silicon layer (9) over the substrate (1) and over the gate structure as shown in Figs. 12A-12B and as described in paragraphs [0136] to [0138]. The silicon layer includes epitaxial portions (10) and amorphous portions (9) as shown in Fig. 12C and as described in paragraphs [0139] to [0143]. The amorphous portions (9) are then removed by selectively etching with respect to the

Art Unit: 2813

epitaxial silicon (10) as shown in Fig. 12D and as described in paragraphs [0144] to [0145]. The silicon layer can be in situ germanium doped (which implies a compressively strained channel) or in situ carbon doped (which implies a tensilely strained channel) (see paragraphs [0120] to [0126]). Also, the silicon layer can be in situ doped with mobility enhancing dopants like boron (which implies a PMOS transistor) or phosphorus or arsenic (which implies an NMOS transistor) (see paragraph [0132]).

These are all of the limitations as set forth in claims 1-5, 11-12, 26-28 of the applicant's invention.

7. Claims 1, 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Natzle et al. (US 2004/0097047 A1).

As best understood, "material over the substrate" as claimed in claim 26 is being interpreted to mean material that is directly in contact with the substrate.

Referring to Figs. 6H, 6I and paragraphs [0116] to [0121], Natzle et al. disclose a method for forming MOSFETs that includes blanket depositing a silicon layer over a silicon substrate (32) and over a gate structure (36, 38, 40) that has epitaxial (42D, 42S), amorphous (42W), and polycrystalline (42C) portions as shown in Fig. 6H. The silicon layer can be conductively doped by in situ growth, which implies a mobility enhanced material. Also, as shown in Fig. 6H, some of the amorphous portions (42W) is elevationally over the gate structure (36, 38, 40). The amorphous portions (42W) are

Art Unit: 2813

then selectively removed by etching with respect to the crystallized portions (42D, 42S, 42C) as shown in Fig. 6I.

These are all of the limitations as set forth in claims 1, 26 of the applicant's invention.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 6-8, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizushima et al. (US 2002/0034864 A1) as applied to claims 1, 26 above, and further in view of Hembree et al. (US 6,224,713 B1).

As shown above, Mizushima et al. anticipate claims 1, 26 of the applicant's invention. However, Mizushima et al. do not teach or suggest etching in the presence of sonication (the limitation of claim 6 and of claim 29) using either tetramethylammonium (the limitation of claim 7) or ammonium hydroxide (the limitation of claim 8). Referring to column 4, lines 14-37, Hembree et al. teach liquid etching of silicon using an etchant that can be tetra methyl ammonium hydroxide (TMAH) in combination with ultrasonic waves (i.e. sonication).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Mizushima et al. and Hembree et al. in order to etch the amorphous silicon of Mizushima et al. using TMAH combined with sonication, as taught by Hembree et al. Hembree et al. recognize that the use of TMAH combined with ultrasonic waves advantageously mixes the etchant mixture on a microscopic level and also assists in promoting bubble detachment (also see abstract).

10. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizushima et al. (US 2002/0034864 A1) as applied to claim 1 above, and further in view of Yamazaki (US 6,011,277).

As shown above, Mizushima et al. anticipate claim 1 of the applicant's invention. Mizushima et al. also disclose depositing amorphous silicon by LPCVD at 550 degrees C (see paragraphs [0138] and [0142]). However, Mizushima et al. do not teach or suggest blanket depositing using trisilane (the limitation of claim 9) at a temperature of less than 550 degrees C (the limitation of claim 10). Referring to column 7, lines 6-21, Yamazaki teaches that amorphous silicon can be deposited by LPCVD using trisilane as the silicon source and also depositing at a temperature ranging from 450 to 550 degrees C.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Mizushima et al. and Yamazaki in order to form the amorphous silicon of Mizushima et al. at a temperature



Art Unit: 2813

ranging from 450 to 550 degrees C and using trisilane as the silicon source, as taught by Yamazaki. Yamazaki recognizes that the trisilane can be used as the silicon source for depositing amorphous silicon by LPCVD and that the temperature range of 450 to 550 degrees C is well below the recrystallization temperature of silicon (see column 7, lines 6-21).

11. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizushima et al. (US 2002/0034864 A1) and Hembree et al. (US 6,224,713 B1) as applied to claim 29 above, and further in view of Yamazaki (US 6,011,277).

As shown above, the combination of Mizushima et al. and Hembree et al. has all of the limitations as set forth in claim 29 of the applicant's invention. Mizushima et al. also disclose depositing amorphous silicon by LPCVD at 550 degrees C (see paragraphs [0138] and [0142]). However, this combination does not teach or suggest depositing mobility enhancing material using trisilane at a temperature of less than 550 degrees C (limitations of claim 30). Referring to column 7, lines 6-21, Yamazaki teaches that amorphous silicon can be deposited by LPCVD using trisilane as the silicon source and also depositing at a temperature ranging from 450 to 550 degrees C.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Mizushima et al., Hembree et al., and Yamazaki in order to form the amorphous silicon of Mizushima et al. at a temperature ranging from 450 to 550 degrees C and using trisilane as the silicon source, as taught by Yamazaki. Yamazaki recognizes that the trisilane can be used as

the silicon source for depositing amorphous silicon by LPCVD and that the temperature range of 450 to 550 degrees C is well below the recrystallization temperature of silicon (see column 7, lines 6-21).

12. Claims 13, 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizushima et al. (US 2002/0034864 A1) as applied to claims 1, 26 above, and further in view of applicant's admitted prior art (page 1).

As shown above, Mizushima et al. anticipate claims 1, 26 of the applicant's invention. Mizushima et al. also anticipate the limitation of claim 32 because they teach in situ doping with carbon (see paragraph [0126]).

However, Mizushima et al. lack the steps of removing implanted source/drain regions replacing them with the crystalline film, which are limitations of claims 13, 31. Referring to page 1, lines 8-18, the applicant indicates that it is known in the art to form a strained channel with increased mobility by removing implanted source drain regions and depositing doped epitaxial silicon in their place.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of Mizushima et al. by replacing implanted source/drain regions with doped epitaxial silicon in order to form a transistor with a strained channel, as disclosed by the applicant, because the applicant indicates that this is a known way to increase mobility in the channel of a field effect transistor (see page 1, lines 8-18).

13. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizushima et al. (US 2002/0034864 A1) in view of applicant's admitted prior art (page 1).

Referring to Figs. 12A-12D and paragraphs [0119] to [0149], Mizushima et al. disclose a method for forming MOS transistors that includes forming a gate structure (2, 6, 7, 8) over a substrate (1) and then forming a silicon layer (9) over the substrate (1) and over the gate structure as shown in Figs. 12A-12B and as described in paragraphs [0136] to [0138]. The silicon layer includes epitaxial portions (10) and amorphous portions (9) as shown in Fig. 12C and as described in paragraphs [0139] to [0143]. The amorphous portions (9) are then removed by selectively etching with respect to the epitaxial silicon (10) as shown in Fig. 12D and as described in paragraphs [0144] to [0145]. The silicon layer can be in situ carbon doped to create strain between the substrate and the silicon layer (see paragraph [0126]). These are limitations as set forth in claims 19-21 of the applicant's invention.

However, Mizushima et al. lack the steps of removing implanted source/drain regions on either side of the gate structure and replacing them with the crystalline film, which are limitations of claim 19.

Referring to page 1, lines 8-18, the applicant indicates that it is known in the art to form a strained channel by removing implanted source drain regions and depositing doped epitaxial silicon in their place.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of Mizushima et al. by replacing

Art Unit: 2813

implanted source/drain regions with doped epitaxial silicon in order to form a transistor with a strained channel, as disclosed by the applicant, because the applicant indicates that this is a known way to increase mobility in the channel of a field effect transistor (see page 1, lines 8-18).

14. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizushima et al. (US 2002/0034864 A1) and applicant's admitted prior art (page 1) as applied to claim 21 above, and further in view of Hembree et al. (US 6,224,713 B1).

As shown above, the combination of Mizushima et al. and applicant's admitted prior art has all of the limitations as set forth in claim 21 of the applicant's invention. However, this combination does not teach or suggest etching in the presence of sonication (the limitation of claim 22) using either tetramethylammonium (the limitation of claim 23) or ammonium hydroxide (the limitation of claim 24). Referring to column 4, lines 14-37, Hembree et al. teach liquid etching of silicon using an etchant that can be tetra methyl ammonium hydroxide (TMAH) in combination with ultrasonic waves (i.e. sonication).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Mizushima et al., applicant's admitted prior art, and Hembree et al. in order to etch the amorphous silicon of Mizushima et al. using TMAH combined with sonication, as taught by Hembree et al. Hembree et al. recognize that the use of TMAH combined with ultrasonic waves

Art Unit: 2813

advantageously mixes the etchant mixture on a microscopic level and also assists in promoting bubble detachment (also see abstract).

15. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizushima et al. (US 2002/0034864 A1) and applicant's admitted prior art (page 1) as applied to claim 19 above, and further in view of Yamazaki (US 6,011,277).

As shown above, the combination of Mizushima et al. and applicant's admitted prior art has all of the limitations as set forth in claim 19 of the applicant's invention. Mizushima et al. also disclose depositing amorphous silicon by LPCVD at 550 degrees C (see paragraphs [0138] and [0142]). However, this combination does not teach or suggest depositing a silicon layer using trisilane at a temperature of less than 550 degrees C (limitations of claim 25). Referring to column 7, lines 6-21, Yamazaki teaches that amorphous silicon can be deposited by LPCVD using trisilane as the silicon source and also depositing at a temperature ranging from 450 to 550 degrees C.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Mizushima et al., applicant's admitted prior art, and Yamazaki in order to form the amorphous silicon of Mizushima et al. at a temperature ranging from 450 to 550 degrees C and using trisilane as the silicon source, as taught by Yamazaki. Yamazaki recognizes that the trisilane can be used as the silicon source for depositing amorphous silicon by LPCVD and that the temperature range of 450 to 550 degrees C is well below the recrystallization temperature of silicon (see column 7, lines 6-21).

### ***Response to Arguments***

16. Applicant's arguments, see page 6, received 12 May 2006, with respect to the rejections of claims 1-13 have been fully considered and are persuasive. It is agreed that Steele et al. lack the claim feature of forming an amorphous mobility enhancing film as required by independent claim 1. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Mizushima et al. and in view of Natzle et al.

Regarding claims 9-10, the prior Office did include a prior art rejection of these claims on pages 10-11 (item number 12).

17. Applicant's arguments with respect to claims 19-32 (see page 7) have been considered but are moot in view of the new grounds of rejection.

### ***Conclusion***

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

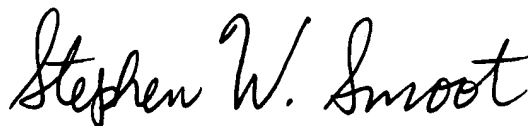
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone

Art Unit: 2813

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SWS

A handwritten signature in black ink that reads "Stephen W. Smoot". The signature is fluid and cursive, with the first letters of each word being capitalized and prominent.

**STEPHEN W. SMOOT**  
**PRIMARY EXAMINER**